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EXAMINER

HANNAHER, CONSTANTINE

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 19

Application Number: 09/667,826
Filing Date: September 21, 2000
Appellant(s): CANNATA ET AL.

Kevin P. Correll¹
For Appellant

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EXAMINER'S ANSWER

This is in response to the appeal brief filed August 26, 2002. This brief is timely filed in reply to the Notification of Non-Compliance with 37 CFR 1.192(c) mailed August 1, 2002. Appellant's

representative and a check of the public PAIR system confirm that the maintenance fee due by the 4 year anniversary of the patenting date of United States Patent 5,811,808 sought to be reissued (that is, by September 23, 2002) has been paid.

(0) Citations of Statute

The text of those sections of Title 35, U.S. Code not included in this answer can be found in a prior Office action (final action of January 17, 2002).

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

¹ The Examiner is led to understand that this attorney is no longer associated with the prosecution of this reissue application. The assistance of Harry Smith (Reg. No. 32,493) in clarifying the status of the application sought to be reissued is appreciated.

(7) Grouping of Claims

Appellant's brief includes a statement that claims (all except as noted) do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

US 4,752,694 A	Hegel, Jr. et al.	06-1988
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(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 40-50 and 52-58 are rejected under 35 U.S.C. 251 as being an improper recapture of broadened claimed subject matter surrendered in the application for the patent upon which the present reissue is based. See *Hester Industries, Inc. v. Stein, Inc.*, 142 F.3d 1472, 46 USPQ2d 1641 (Fed. Cir. 1998); *In re Clement*, 131 F.3d 1464, 45 USPQ2d 1161 (Fed. Cir. 1997); *Ball Corp. v. United States*, 729 F.2d 1429, 1436, 221 USPQ 289, 295 (Fed. Cir. 1984). A broadening aspect is present in the reissue which was not present in the application for patent. The record of the application for the patent shows that the broadening aspect (in the reissue) relates to subject matter that applicant previously surrendered during the prosecution of the application. Accordingly, the narrow scope of the claims in the patent was not an error within the meaning of 35 U.S.C. 251, and the broader scope surrendered in the application for the patent cannot be recaptured by the filing of the present reissue application.

The reissue claims 40, 41, 42, 43, 52, and 58 delete a limitation ("parallel connected") from the patent claims. Therefore, the reissue claims are broader than the patent claims in the aspect of the electrical connection of the plurality of circuit elements. The broader aspect of the reissue claims

relates to subject matter that applicant previously surrendered during the prosecution of the original application. The limitation (“parallel connected”) omitted in the reissue claims was present in the claims of the original application (at least claims 2-4, 8, 24, 26, 37, 42, 44, and 45). The examiner’s reasons for allowance in the original application stated that it was that limitation (“the means for correcting specified by independent claim 2, 24, 33 or 37” where the means for correcting specified a correction circuit including a plurality of parallel connected circuit elements and means for selectively electrically connecting said circuit elements into the detector readout circuit in response to stored offset correction values) which distinguished over a potential application of references Lung and Masarik *et al.* Applicant did not present on the record a counter statement or comment as to the examiner’s reasons for allowance, and permitted the claims to issue. The omitted limitation is thus established as relating to subject matter previously surrendered. MPEP § 1412.02.

The reissue claim 53 deletes a limitation (“capacitors”) from the patent claims. Therefore, the reissue claims are broader than the patent claims in the aspect of the electrical connection between the sample node and a reference voltage. The broader aspect of the reissue claims relates to subject matter that applicant previously surrendered during the prosecution of the original application. The limitation (“capacitors”) omitted in the reissue claims was present in the claims of the original application (claim 32). The examiner’s reasons for allowance in the original application stated that it was that limitation (“the means for correcting specified by independent claim 2, 24, 33 or 37” where the means for correcting specified a plurality of capacitors connected between said sample node and a reference voltage and a corresponding plurality of switches coupled in series with each respective capacitor and said reference voltage) which distinguished over a potential application of references Lung and Masarik *et al.* Applicant did not present on the record a counter statement or

comment as to the examiner's reasons for allowance, and permitted the claims to issue. The omitted limitation is thus established as relating to subject matter previously surrendered. MPEP § 1412.02.

Claims 40-50 and 52-58 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification does not describe an infrared imaging system or an infrared focal plane array in which the circuit elements of the correction circuit in the means for separately correcting offsets in the detection signals are not parallel connected. Note the illustrations of the claimed subject matter as offset correction circuit **220**. A plurality of circuit elements (the capacitors **224**) and switches **228** are parallel connected in Figs. **3B** and **3C**. A plurality of circuit elements (the constant current sources **400**) and switches **228** are parallel connected in Figs. **10** and **11**. A plurality of circuit elements (the constant current sources **600**) and switches **610** are parallel connected in Fig. **12**. Note the repeated description of the correction circuit as a plurality of circuit elements which are "parallel connected": column 3, lines 59, 62, and 66; column 13, line 15; column 16, line 49; and, column 17, line 20. No other form of electrical connection for the plurality of circuit elements is disclosed. The original specification demonstrates, to one skilled in the art, an absence of disclosure sufficient to indicate that a patentee could have claimed the subject matter.

The specification does not describe an infrared focal plane array in which the means for correcting the analog detection signal does not comprise capacitors or parallel connected constant current sources. Note the illustrations of the claimed subject matter as offset correction circuit **220**. A plurality of capacitors **224** are connected between the sample node **222** and a reference voltage V_R in Figs. **3B** and **3C**. A plurality of parallel connected constant current sources **400** are connected

between the sample node **222** and a reference voltage V_R in Figs. **10** and **11**. A plurality of parallel connected constant current sources **600** are connected between the sample node **222** and a reference voltage V_R in Fig. **12**. Note the repeated description of the correction circuit as capacitors or parallel connected constant current sources: column 3, lines 62-64; column 13, line 15; column 16, line 49; and, column 17, line 20. No other type of circuit elements is disclosed. Since claim 53 differs from claim 58 only in the inclusion of a method of operation at the end and process limitations cannot serve to impart patentability to structures, and claim 58 recites the constant current sources, the principle of claim differentiation demands that the means for correcting in claim 53 be the disclosed plurality of capacitors. The original specification demonstrates, to one skilled in the art, an absence of disclosure sufficient to indicate that a patentee could have claimed the subject matter.

Claims 1, 5, 21, 22, 40, 42, and 48 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hegel, Jr. *et al.* (US004752694A).

With respect to independent claim 1, Hegel, Jr. *et al.* discloses an infrared imaging system (Fig. **1**) comprising an infrared focal plane array **10** comprising a plurality of infrared detector elements (*e.g.*, **11**) arranged in an array, a readout circuit coupled to the plurality of detector elements **11** and comprising means for biasing the plurality of detector elements **11** (from bias source at **A**) so as to provide separate detection signals (at node **B**) corresponding to each detector element **11** in the array in response to incident infrared radiation **75** and means for separately correcting offsets in the detection signals provided from the plurality of (detector) elements in the (focal plane) array to compensate for nonuniformities in the detector elements (column 1, lines 11-13) wherein the means for (separately) correcting comprises a correction circuit including a plurality of circuit elements (FETs **14**, **15**, **16**) and means **60** for selectively electrically connecting the circuit elements **14**, **15**, **16** into the detector readout circuit in response to stored offset correction values (arriving along

conductor **73**), and output means **51** for providing the corrected detection signals as an output of the focal plane array, means **70** for storing a plurality of offset correction values corresponding to the plurality of detector elements **11**, and means **71, 72** for providing the offset correction values to the means for (separately) correcting. Column 3, lines 29-52. The plurality of circuit elements **14, 15, 16** in the infrared imaging system of Hegel, Jr. *et al.* are parallel connected (Fig. 1).

With respect to dependent claim 5, the means for selectively (electrically) connecting **60** in the infrared imaging system of Hegel, Jr. *et al.* comprises a plurality of switches **A, B, C** equal in number to the plurality of circuit elements **14, 15, 16** and connected in series therewith (Fig. 1) at nodes **17, 18, and 19**.

With respect to dependent claim 21, the infrared imaging system of Hegel, Jr. *et al.* further comprises timing means (delivering the "clock input") for providing timing signals to the readout circuit.

With respect to dependent claim 22, the readout circuit in the infrared imaging system of Hegel, Jr. *et al.* further comprises offset correction logic means **62** for controlling the means for correcting in response to the timing signals.

With respect to independent claim 40, Hegel, Jr. *et al.* discloses an infrared imaging system (Fig. 1) comprising an infrared focal plane array **10** comprising a plurality of infrared detectors elements (*e.g.*, **11**) arranged in an array, a readout circuit coupled to the plurality of detector elements **11** and comprising means for biasing the plurality of detector elements **11** (from bias source **A**) so as to provide separate detection signals (at node **B**) corresponding to each detector element **11** in the array in response to incident infrared radiation **75** and means for separately correcting offsets in the detection signals provided from the plurality of (detector) elements in the (focal plane) array to compensate for nonuniformities in the detector elements (column 1, lines 11-13) wherein the means

for (separately) correcting comprises a correction circuit including a plurality of circuit elements (FETs **14, 15, 16**) and means **60** for selectively electrically connecting the circuit elements **14, 15, 16** into the detector readout circuit in response to stored offset correction values (arriving along conductor **73** from the storage in **70**), and output means **51** for providing the corrected detection signals as an output of the focal plane array, means **70** for storing a plurality of offset correction values corresponding to the plurality of detector elements **11**, and means **71, 72** for providing the offset correction values to the means for (separately) correcting. Column 3, lines 29-52.

With respect to dependent claim 42, the means for selectively (electrically) connecting **60** in the infrared imaging system of Hegel, Jr. *et al.* comprises a plurality of switches **A, B, C** equal in number to the plurality of circuit elements **14, 15, 16** and connected in series therewith (Fig. 1) at nodes **17, 18, and 19**.

With respect to dependent claim 48, the infrared imaging system of Hegel, Jr. *et al.* further comprises timing means (delivering the "clock input") for providing timing signals to the readout circuit.

Claims 6, 7, 12, 13, 15, 19, 24, 25, 44, 45, 46, 47, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hegel, Jr. *et al.* (US004752694A).

With respect to dependent claim 6, the memory **70** in the infrared imaging system of Hegel, Jr. *et al.* is a digital memory (column 3, lines 32-33) but there is no requirement that the digital data number stored therein is specifically in base 2. The choice of base for the storage of numbers is entirely within the ordinary skill in the art. Binary is a well-known choice of base in view of the ready availability of hardware and software of effective performance in handling numbers with a base of 2. Note the discussion of an alternative embodiment at column 4, lines 63-68 in which the number 65,536 is exactly 2^{16} which is highly suggestive that digital memory **70''** stores the numbers in base 2.

With respect to dependent claim 7, there is a separate digital data number for each detector element in the infrared imaging system of Hegel, Jr. *et al.* (column 3, lines 36-39).

With respect to dependent claim 12, the formation of the elements of the infrared imaging system illustrated by Hegel, Jr. *et al.* in Fig. 1 on a single monolithic integrated circuit chip would have been obvious to one of ordinary skill in the art at the time the invention was made in view of the known advantages of miniaturization (column 1, lines 33-36).

With respect to dependent claim 13, the detector elements 11 in the infrared imaging system of Hegel, Jr. *et al.* are bolometers (column 1, line 11). The specific identification of "micro" bolometers is a choice within the ordinary skill in the art depending on the size of the resistive sensors. A micrometer is a millionth of a meter.

With respect to dependent claim 15, the infrared imaging system of Hegel, Jr. *et al.* comprises a fixed voltage from the source at node A coupled to the detector elements.

With respect to dependent claim 19, the output means 51 in the infrared imaging system of Hegel, Jr. *et al.* is illustrated schematically. The inclusion of buffers therein is a choice which would have been obvious to one of ordinary skill in the art at the time the invention was made in view of the circuit protection afforded thereby.

With respect to dependent claim 24, the output means 51 in the infrared imaging system of Hegel, Jr. *et al.* is illustrated schematically. The inclusion of means for analog to digital converting and providing corresponding image data is a choice which would have been obvious to one of ordinary skill in the art at the time the invention was made in view of the desire for manipulation of detector element signal data and the desire to view the infrared radiation incident on the array.

With respect to dependent claim 25, the provision of a memory for the image data delivered by output means 51 in the infrared imaging system of Hegel, Jr. *et al.* would have been obvious to

one of ordinary skill in the art at the time the invention was made in view of the desire for later transmission or non real time processing thereof.

With respect to dependent claim 44, the output means **51** in the infrared imaging system of Hegel, Jr. *et al.* is illustrated schematically. The inclusion of means for analog to digital converting and providing corresponding image data is a choice which would have been obvious to one of ordinary skill in the art at the time the invention was made in view of the desire for manipulation of detector element signal data and the desire to view the infrared radiation incident on the array.

With respect to dependent claim 45, the detector elements **11** in the infrared imaging system of Hegel, Jr. *et al.* are bolometers (column 1, line 11). The specific identification of "micro" bolometers is a choice within the ordinary skill in the art depending on the size of the resistive sensors. A micrometer is a millionth of a meter.

With respect to dependent claim 46, the memory **70** in the infrared imaging system of Hegel, Jr. *et al.* is a digital memory (column 3, lines 32-33) but there is no requirement that the digital data number stored therein is specifically in base 2. The choice of base for the storage of numbers is entirely within the ordinary skill in the art. Binary is a well-known choice of base in view of the ready availability of hardware and software of effective performance in handling numbers with a base of 2. Note the discussion of an alternative embodiment at column 4, lines 63-68 in which the number 65,536 is exactly 2^{16} which is highly suggestive that digital memory **70''** stores the numbers in base 2.

With respect to dependent claim 47, the formation of the elements of the infrared imaging system illustrated by Hegel, Jr. *et al.* in Fig. 1 on a single monolithic integrated circuit chip would have been obvious to one of ordinary skill in the art at the time the invention was made in view of the known advantages of miniaturization (column 1, lines 33-36).

With respect to dependent claim 50, the output means **51** in the infrared imaging system of Hegel, Jr. *et al.* is illustrated schematically. The inclusion of buffers therein is a choice which would have been obvious to one of ordinary skill in the art at the time the invention was made in view of the circuit protection afforded thereby.

(11) Response to Argument

The tests set forth in *Hester* at pages 1648-1650 have been applied properly and there is no material narrowing of the claims in other respects that would save them under the principle found in *Mentor Corp. v. Coloplast, Inc.*, 998 F.2d 992, 27 USPQ2d 1521 (Fed. Cir. 1993). Application of the recapture rule as a three-step process remains a valid procedure. *See Pannu v. Storx Instruments Inc.*, 59 USPQ2d 1597 (Fed. Cir. 2001).

Recourse to example (A) of MPEP § 1412.02 is not available to the appellant since no aspect of the means for correcting was argued to make the application claims allowable over a rejection or objection made in the application. Similarly, there is no recourse to example (B) of MPEP § 1412.02 since no aspect of the means for correcting was amended to make the application claims allowable over a rejection or objection made in the application. The Examiner indicated allowability for claims 2, 24, 33, and 37 if rewritten in independent form in the Office action mailed March 7, 1997. The only valid analytical tool is example (C).

The Examiner's statement of reasons for allowance as made in the attachment to the Notice of Allowability mailed December 9, 1997 is not a general "boiler plate" sentence of the type exemplified by MPEP § 1412.02, example (A) because it is directed to a *specific* limitation and to *specific* claims as opposed to a general statement regarding the claims as a whole:

the prior art of record fails to teach or fairly suggest an infrared imaging system or focal plane array having in combination with the other required elements, the means for

correcting specified by independent claim[s] 2, 24, 33 or 37. Claims not addressed are allowable by virtue of their dependency.

Claims 2, 24, 33, and 37 became patent claims 1, 26, 27, and 35. Since the specific limitation of a means for correcting *as specified by these claims* as plainly stated by the allowing examiner is not found in independent claims 40, 52, 53, and 58, the limitation that the examiner's statement of reasons for allowance stated distinguished over a potential combination of references is no longer present in these added claims (it has been omitted and a means for correcting **not of the type** specified in application claims 2, 24, 33, or 37 has been substituted therefor).

At the most general level, claim 40 recites an infrared imaging system. The system comprises an infrared focal plane array. The array comprises detector elements and a readout circuit. The readout circuit comprises means for biasing, means for separately correcting offsets, means for storing, and means for providing. The means for (separately) correcting offsets comprises a correction circuit, means for selectively electrically connecting, and an output means. The correction circuit includes a plurality of circuit elements. At what degree of specificity does the parallel connection of the plurality of circuit elements become established as a limitation which distinguishes over a potential combination of references? Of the one limitation to the system, of the two limitations to the array, of the four limitations to the readout circuit, the examiner in the allowance mentioned one: the means for correcting specified in claim[s] 2, 24, 33, or 37. Not just "a" means for correcting as stated by Appellant at page 22, *the* means for correcting *specified* by the enumerated claims. *That* means for correcting (as specified in claims 2, 24, 33, and 37) is not recited in claim 40 (or in claim 53), because of *its* three limitations, one has been amended. How is this insufficiently specific? The Examiner disagrees that the reasons for allowance are a general "boiler plate" sentence but does not find any guidance in MPEP 1412.02 or *Hester* as to how narrowly the limitation must

be identified to invoke the principles therein. It should be apparent that the allowing examiner made no particular comment about the system, the array, the detector elements, the means for biasing, the means for storing, or the means for providing, yet it is the readout circuit's means for separately correcting--the one thing the examiner did mention in the reasons for allowance--that appellant has chosen to amend in reissue.

While acknowledging the Examiner's listing of those portions of the specification and the those views which show a parallel connection, Appellant insists that this is only a preferred implementation but is unable to identify a single phrase, sentence, or view which would suggest to one skilled in the art any other connection. The argument regarding the situation where $N=0$ is completely spurious because the claims (even claims 40, 52, 53, and 58) demand a plurality of circuit elements, so this situation is *outside* the scope of the claims. This is important regarding the argument on page 25: N cannot be zero not least because the switches 228 are *not* a part of the plurality of circuit elements recited in the claim, they are the means for selectively electrically connecting! (Even more specifically, in view of appellant's arguments regarding the application of 35 U.S.C. 112, sixth paragraph, the capacitors 224 or the current sources 500 are not structure, material, or acts which correspond to the recitation of "means for selectively electrically connecting." Only switches 228 qualify. See column 3, lines 62-65 which appellant relies on in attempting to distinguish Hegel, Jr. *et al.*: "The plurality of parallel connected circuit elements may comprise a plurality of capacitors or constant current sources. The means for selectively connecting may comprise a plurality of switches....") The argument regarding higher values of N is bizarre, as it suggests that a correction circuit in which none of the circuit elements were connected (as by leaving all of the switches S open) would not be an infringement of the claim! Even one moderately skilled in the art should recognize in the context of an infrared imaging system of the type recited that making and selling a

correction circuit of the type described, illustrated, and claimed should be an infringement even if all of the switches are left open leaving the circuit elements literally not “connected.” Perhaps the figures should be objected to since they show all the switches open and thus do not, in view of the argument presented, illustrate any connection of the circuit elements, parallel or otherwise (and thus do not show the claimed subject matter)? The parallel connection described in the patent is valid regardless of the state of the switches **228**. The argument based on an insufficient understanding of the scope and contents of the claims is not persuasive.

With respect to independent claim 1, appellant devotes some space to establishing that claim 1 should be analyzed according to what corresponds to the guidelines set forth in MPEP § 2181 and then asserts (page 6) that, because the specification identifies capacitors or constant current sources as the plurality of circuit elements called for by claim 1 as one element of a “means for separately correcting offsets,” the Examiner is precluded from using Hegel, Jr. *et al.* against the claim. Why? Apparently because the plurality of circuit elements in the applied reference are transistors **14, 15, 16**. Note carefully, however, that the plurality of circuit elements are included in an element (“a correction circuit”) which has none of the qualifications for treatment under any “means for” test. Lacking a use of “means for,” lacking any modification by functional language (as the compensation for nonuniformities in the detector elements is explicitly the function of the “means for separately correcting offsets”), and presenting sufficient structure, material or acts (“including a plurality of parallel connected circuit elements”), the limitation in claim 1 to a correction circuit cannot be construed as a means-plus-function limitation. There is no barrier, therefore, to identifying the transistors **14, 15, 16** in Hegel, Jr. *et al.* as the plurality of parallel connected circuit elements included in a correction circuit as called for by the claim.

There can be no reasonable argument that the switches **60** in Hegel, Jr. *et al.* do not correspond to the recited means for selectively electrically connecting (the second element of the correction circuit) since the corresponding structure in appellant's specification is switches **228**. There can be no reasonable argument that the node **B** does not correspond to the recited output means for providing the corrected detection signals (the third and final element of the correction circuit) since the corresponding structure in appellant's specification is node **222**. As memory **70** in Hegel, Jr. *et al.* corresponds to the structure of memory **26** and conductor **73** corresponds to conductors **138**, there is no element of the recited "means for separately correcting offsets" that does not find correspondence to a structure in Hegel, Jr. *et al.* even in light of and consistent with the written description of the invention in the application as emphasized by appellant.

It may be noted that appellant requires the plurality of circuit elements in claim 1 to be a plurality of capacitors or constant current sources for the purposes of 35 U.S.C. 112, sixth paragraph, but denies that they must be parallel connected or capacitors for the purposes of 35 U.S.C. 112, first paragraph.

Furthermore, there is no adding or subtracting recited in claim 1, so the presence or absence thereof in the applied reference is irrelevant. Appellant has failed to identify which "means for" element of the claim must include this act of addition or subtraction. The argument cannot be persuasive.

The Board will note that the Examiner does not refer to the FETs **44**, **45**, **46** of Hegel, Jr. *et al.* in applying the reference to the claim. Why? Because they do not provide the variations in applied bias from node **A** to make the resistance between **A** and **B** the same regardless of the characteristics of the individual detector elements, as fully explained by the applied reference from column 2, line 56 to column 3, line 52, and thus compensating for nonuniformities in the operation of the detector

elements **11**. Accordingly, the electrical short circuit established by the FETs **44, 45, 46** does not relate to any claim element, and the argument cannot be persuasive.

Again, on page 8, appellant relies on the specification and drawings to attempt a refutation of the rejection of claim 1. Since addition or subtraction, direct (as emphasized on page 7 and repeated on page 9) or otherwise, is not a part of the claim, this argument cannot be persuasive.

Appellant makes more arguments regarding the operation of the detector array of Hegel, Jr. *et al.* on page 9. Since the argument does not relate to claim limitations, and does not correspond to the description Hegel, Jr. *et al.* provide for the operation of their array, the argument cannot be persuasive.

With respect to dependent claim 5, since switches **60** in Hegel, Jr. *et al.* correspond *exactly* to the structure of switches **228** in the disclosure, the argument for claim 5 relies on the limitations of claim 1 (see pages 9 and 10). Accordingly, the argument required by 37 CFR 1.192(c)(7) does not, in fact, exist for dependent claim 5.

With respect to dependent claim 21, does the “clock input” of Hegel, Jr. *et al.* provide timing signals to the readout circuit? In view of the synchronization afforded thereby, the answer is yes. Appellant is happy to point out the connection of sequencer **62** to switches **61** (page 10) but does not mention the connection to switches **60** which do control the readout (by determining which detector element gets read out) and control the offset correction (by adjusting the resistance of circuit elements **14, 15, 16** in accordance with data from memory **70** also connected to sequencer **62**).

With respect to dependent claim 22, does sequencer **62** control the means for correcting (circuit elements **14, 15, 16**, switches **60**, and output node **B**) in response to the timing signals from the clock input? Yes, it does (column 2, lines 50-52).

With respect to independent claim 40, since this claim differs from claim 1 only in what constitutes the “correction circuit,” the arguments inherit all the flaws of the arguments regarding claim 1 and will not be repetitiously addressed. It may be noted that attempting to define offset as an addition or subtraction (page 12) is not a requirement of any claim. It may also be noted that the “stored offset correction values” of the claim do not get added or subtracted to or from any detector signal. Instead, the stored offset correction values arrive along conductors **138** in Fig. **3B** and control which of switches **228** get closed and which are left open so as to adjust the current flow between V_R and node **222**. It is this current flow, exactly corresponding to the current flow between node **A** and across circuit elements **14, 15, 16** in Hegel, Jr. *et al.*, that adjusts (offsets) the detector signal which would otherwise be delivered to the output node.

With respect to dependent claims 42 and 48, the arguments presented are no more persuasive than those applied regarding claims 5 and 21.

With respect to dependent claim 6, since the memory **70** in Hegel, Jr. *et al.* corresponds to the structure of memory **26** in the disclosure, the argument for claim 6 relies on the limitations of claim 1 (see page 14). Accordingly, the argument required by 37 CFR 1.192(c)(7) does not, in fact, exist for dependent claim 6.

With respect to dependent claim 12, the argument relies on the limitations of claim 1, since there is no issue between the Examiner and the appellant regarding the obviousness of single monolithic integration for any arbitrary circuit. Accordingly, the argument required by 37 CFR 1.192(c)(7) does not, in fact, exist for dependent claim 12.

With respect to dependent claim 13, the argument relies on the limitations of claim 1, since there is no issue between the Examiner and the appellant regarding the obviousness of naming the

bolometers (column 1, lines 11-13) of Hegel, Jr. *et al.* Accordingly, the argument required by 37 CFR 1.192(c)(7) does not, in fact, exist for dependent claim 13.

With respect to dependent claim 15, the argument relies on the limitations of claim 1, since there is no issue between the Examiner and the appellant regarding the obviousness of whether the battery attached to node A in the Fig. 1 of Hegel, Jr. *et al.* is a fixed voltage source. Accordingly, the argument required by 37 CFR 1.192(c)(7) does not, in fact, exist for dependent claim 15.

With respect to dependent claim 19, it is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by appellant. There is no issue between the Examiner and the appellant that “output buffers” in the abstract are a known circuit element, so the imperative of, for example, *In re Royka*, that all claim limitations must be taught or suggested by the prior art has been met for this claim. Appellant disagrees regarding the obviousness of such a modification.

With respect to dependent claim 24, there should not be an issue between the Examiner and the appellant that “means for analog to digital converting” in the abstract are a known circuit element, especially as Hegel, Jr. *et al.* is fully aware of means for digital to analog converting (see element 71). The readout supplied by element 51 may very well be in the analog domain, but for at least the reasons given by the Examiner in explaining the rejection, and others of transmission over distances or display on digitally controlled monitors or as input to algorithmic target trackers and the like, the obviousness of adding this known circuit element to the infrared imaging system of Hegel, Jr. *et al.* is maintained.

With respect to dependent claim 25, there should not be an issue between the Examiner and the appellant that a memory for storing image data in the abstract is a known circuit element. For at least the reasons given by the Examiner in explaining the rejection, the obviousness of adding such a

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memory is maintained. Would one of ordinary skill in the art, confronted by the continually changing information regarding radiation image 75 ending up in circuit 51, just throw it away?

With respect to dependent claims 44 and 45 and 46 and 47 and 50, the arguments presented are no more persuasive than those applied regarding claims 24 and 13 and 6 and 12 and 19.

(12) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



Constantine Hannaher
Primary Examiner

ch
October 29, 2002

Conferees
Olik Chauduri *OC*
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